REMARKS/ARGUMENT

Claims 2-21 are pending. Claims 2-21 have been finally rejected. The drawings and claims are objected to. Claims 4 and 17-21 stand rejected under 35 U.S.C. § 112, second paragraph as indefinite. Claims 2, 4-7, 10, 14, 16-17, 19 and 21 stand rejected under 35 U.S.C. § 102(b). Claims 3 and 11-12 stand rejected under 35 U.S.C. § 103(a).

By this amendment, Applicant amends claims 2, 4, 7 and 17 to remove the objections and rejections thereon. Further, Applicant respectfully traverses the rejections under §§ 102 and 103.

In paragraph 3 of the Office Action, the drawings are objected to. Specifically, the Office Action states that the drawings fail to show that "the control means is constituted by a second n-bit shift register for shifting a ramp-up/down signal through successive bit stages under control of a shift clock for the first n-bit shift register." This limitation is shown in, by way of non-limiting example, Fig. 2. Fig. 2 shows that the control circuit is a n-bit shift register that receives and shifts a ramp-up/down signal. This is confirmed in the specification: "An example of the internal construction of the control circuit 101 will now be described with reference to Fig. 2. Referring to the Figure, the control circuit 101 includes a shift registers 101 comprising n bit registers 101-1 to 101-n which receives a ramp-up/-down signal and progressively shifts the input signal at shift timings on the basis of the clock signal." (Page 9, lines 16-22, emphasis added.) Thus, the drawings clearly show a control means "constituted by a second n-bit shift register for shifting a ramp-up/down signal through successive bit

stages under control of a shift clock for the first n-bit shift register." Withdrawal of the objections to the drawings is thus respectfully requested.

In paragraph 4 of the Office Action, claims 2, 10 and 17 are objected to. The Office Action advises that the Applicant replace the term "FIR" with "Finite Impulse Response (FIR)." Applicant hereby amends the claims in accordance with the Examiner's advice.

In paragraph 6 of the Office Action, claims 4 and 17-21 are rejected under 35 U.S.C. § 112, second paragraph. Claim 4 is rejected as lacking antecedent basis. Applicant has amended claim 4 to remove the rejection. Claim 17 is rejected as being unclear whether "the FIR filter coefficient circuits [sic, circuit]" refers to coefficient circuits {h1-hn} or input data {d1-dn}. For examination purposes, the Office Action states that it is considered to refer to {d1-dn}. Applicant respectfully submits that the claim is not indefinite as the term "FIR filter coefficient circuit" clearly refers to a coefficient circuit and not data. For example, Fig. 6 shows "a circuit 82 for producing an FIR filter coefficient hi (i being 1 to n)". (Page 16, lines 6-10.) As one skilled in the art would understand that a recitation of "coefficient circuit" is claiming a coefficient circuit, withdrawal of the rejection of claim 17 on this ground is respectfully requested. Claims 18-21 are rejected as dependent on base claim 17. For the reasons given above with respect to claim 17, withdrawal of the rejections of claims 18-21 is respectfully requested. Further, to the extent that the Office Action has rejected claim 17 on this ground, having considered that it refers to input data {d1-dn}, these rejections are erroneously taken and must be withdrawn.

In paragraph 8 of the Office Action, claims 2, 4-7, 10, 14, 16-17, 19 and 21 are rejected under 35 U.S.C. § 102(b) over Hidemitsu, J.P. 411088119A. Applicant respectfully traverses these rejections.

Nowhere does Hidemitsu show, as required by amended claim 2, a FIR filter including a "control means further [] constituted by a second n-bit shift register for shifting a ramp-up/-down signal through successive bit stages under control of a shift clock for the first n-bit shift register." This limitation of claim 2 was previously presented in at least claim 3 and does not require a new search on the part of the Examiner. Hidemitsu fails to teach or suggest a second n-bit shift register for shifting a ramp-up/-down signal through successive bit stages under control of a shift clock for the first n-bit shift register. Indeed, Hidemitsu fails to teach or suggest any ramp-up/-down signal that acts on a data signal. Withdrawal of the rejection of claim 2 is therefore respectfully requested.

Claims 4-7 are also rejected under 35 U.S.C. § 102(b) over Hidemitsu. Claims 4-7 depend from claim 2 and include all of the limitations therein. These claims recite added limitations which, in combination with the limitations of claim 2, are not disclosed in the art of record. Accordingly, withdrawal of the rejections of claims 4-7 is respectfully requested.

Independent claim 10 is rejected under 35 U.S.C. § 102(b) over Hidemitsu. Applicant respectfully traverses this rejection.

Nowhere does Hidemitsu show, as required by claim 10 of the present application, a FIR filter including "an n-bit combining circuit coupled to the first n-bit shift register and coupled to the control circuit, the combining circuit combining the n output

signals of the first n-bit shift register with the n unique control signals of the control circuit, the n-bit combining circuit outputting a combining circuit output signal." Hidemitsu fails to teach or suggest a combining circuit, let alone an n-bit combining circuit. Hidemitsu merely shows switch elements, not combining elements. Switches select either one value or another value, and thus consider one value only. A combining circuit combines signals, and thus considers at least two values. Further, the Office Action rejects claim 10 for having "the similar features cited in claim 1." Claim 1, however, had been cancelled in a previous Amendment and did not recite a combining circuit, so this is an inappropriate rejection. Accordingly, for the above reasons, withdrawal of the rejection of claim 10 is respectfully requested.

Further, claims 14 and 16 are also rejected under 35 U.S.C. § 102(b) over Hidemitsu. Claims 14 and 16 depend from claim 10 and include all of the limitations therein. These claims recite added limitations which, in combination with the limitations of claim 10, are not disclosed in the art of record. Accordingly, claims 14 and 16 are believed to be in a condition for allowance.

Further, claim 17 is also rejected under 35 U.S.C. § 102(b) over Hidemitsu. Applicant respectfully traverses this rejection.

Nowhere does Hidemitsu show, as required by claim 17 of the present application, a FIR filter including "a switch coupled to the control circuit, coupled to the fixed value circuit and coupled to the FIR filter coefficient circuit, each switch selecting either the fixed value or the FIR filter coefficient depending upon the control circuit output signal,

outputting a switch selection output." Hidemitsu fails to teach or suggest a switch that can select a FIR filter coefficient. None of Figures 1, 7 and 11 of Hidemitsu show that a FIR filter coefficient value is an input to any of its switches. The inputs for switches shown in Hidemitsu are either switching between the data and 0 (Figure 1), or switching between the data and a code converter which merely appears to invert the value of the delay element (Figure 7) and Figure 11 does not disclose any switches. Thus, Hidemitsu nowhere teaches or suggests a switch that can select "either the fixed value or the FIR filter coefficient", as required by claim 17 of the present invention. Withdrawal of the rejection on claim 17 is respectfully requested.

Claims 19 and 21 are also rejected under 35 U.S.C. § 102(b) over Hidemitsu. Claims 19 and 21 depend from claim 17 and include all of the limitations therein. These claims recite added limitations which, in combination with the limitations of claim 17, are not disclosed in the art of record. Accordingly, withdrawal of the rejections of claims 19 and 21 are respectfully requested.

In Paragraph 10 of the Office Action, claims 3 and 11-12 are rejected under 35 U.S.C. § 103(a) as obvious over Hidemitsu in view of Shinde, U.S. Patent No. 6,192,386. Applicant respectfully traverses these rejections.

Specifically, the Office Action acknowledges that Hidemitsu does not disclose that the n switch means are "each an AND gate for receiving the outputs of the corresponding bit stages of the first and second n-bit shift registers as respective inputs." Shinde is cited for the proposition of using AND gates for switching means. With respect to claim 3, however,

nowhere do Hidemitsu or Shinde show or suggest using AND gates to process a ramp-up/-down signal from a second n-bit shift register. There is no second shift register in Hidemitsu or Shinde. The Office Action identifies a clock signal (CLK2) in Shinde as being the second shift register. This is the second clock signal, not second shift register. Hidemitsu and Shinde fail to teach or suggest a second shift register. Thus, the prior art references, even if combined, fail to teach or suggest all the claim limitations. As such, the Office Action has failed to make out a prima facie case of obviousness. M.P.E.P. § 2143. Withdrawal of the rejection of claim 17 is respectfully requested.

Claims 11-12 are also rejected under 35 U.S.C. § 103 over Hidemitsu and Shinde. Claims 11-12 depend from claim 10. For the reasons given above, Shinde does not cure any deficiency of Hidemitsu with respect to claim 10. Thus, claims 11-12 are patentable over the combination of Hidemitsu and Shinde. Withdrawal of the rejections of claims 11-12 are respectfully requested.

Claims 8-9, 13, 15, 18 and 20 are rejected under 35 U.S.C § 103 over Hidemitsu in view of Shinde in view of Applicant's purported admitted prior art. Applicant respectfully traverses these rejections.

Specifically, the Office Action cites pages 6-7 of Applicant's disclosure as admitted prior art curing the deficiencies of Hidemitsu and Shinde. However, pages 6-7 describe Applicant's invention, not any admitted prior art. Page 6-7 are found in Applicant's Summary of the Invention. Withdrawal of the rejection of claims 8-9 is respectfully requested.

Claims 13, 15, 18 and 20 are also rejected under 35 U.S.C. § 103 over Hidemitsu and Shinde in view of Applicant's purported admitted prior art. The Office Action states that claims 13, 15, 18 and 20 have similar features as those in claims 8-9. Without conceding that the features are similar, Applicant submits that claims 13, 15, 18 and 20 are patentable over Hidemitsu, Shinde and Applicant's purported admitted prior art for the reasons given with respect to claim 3. Withdrawal of the rejections of claims 13, 15, 18 and 20 is respectfully requested.

Applicant has amended claims 2, 4, 7 and 17 to remove the objections and rejections thereon. Further, Applicant has shown that the pending claims are patentable under 35 U.S.C. §§ 102 and 103 over the cited prior art. In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance and such action is earnestly solicited.

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Respectfully submitted,

By 

Michael J. Scheer
Registration No.: 34,425
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
1177 Avenue of the Americas
41st Floor
New York, New York 10036-2714
(212) 835-1400
Attorney for Applicant